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ABSTRACT OF THE DISCLOSURE

An embedded semiconductor product employs a first isolation trench and first isolation region formed therein adjoining a logic cell active region of a semiconductor substrate. The embedded semiconductor product also employs a second isolation trench and second isolation region formed therein adjoining a memory cell active region of the semiconductor substrate. The second isolation trench is deeper than the first isolation trench such that a storage capacitor whose capacitor plate is embedded at least in part within the second isolation region may be formed with enhanced capacitance.